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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,904	01/24/2001	Lap-Wai Chow	B-3964 618029-8	4228

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EXAMINER
NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/768,904	Applicant(s) CHOW ET AL.	
	Examiner Joseph Nguyen	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "a metal plug contact disposed outside a contact region" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8, 17-18, 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Scott et al.

Regarding claim 1, Scott et al discloses on figure 6 a semiconductor device adapted to prevent and/or thwart reverse engineering comprising "field oxide [22] disposed on a semiconductor substrate; a metal plug contact [26] disposed within a contact region and above said field oxide layer; and a metal [32] connected to said metal plug contact".

Regarding claim 2, Scott et al discloses on figure 6 the semiconductor device comprises integrated circuit.

Regarding claim 3, Scott et al discloses on figure 6 the field oxide layer comprises silicon oxide.

Regarding claim 4, Scott et al discloses on figure 6 the integrated circuits further comprise complementary metal oxide semiconductor integrated circuits and bipolar integrated circuits.

Regarding claim 5, Scott et al discloses a method for preventing and /or thwarting reverse engineering comprising steps of "providing a field oxide layer disposed on a semiconductor substrate; providing a metal plug contact [26] disposed within a contact region and above said field oxide layer; and connecting a metal [32] to said metal plug contact".

Regarding claim 6, Scott et al disclose a method on figure 6 the semiconductor device comprises integrated circuit.

Regarding claim 7, Scott et al discloses on figure 6 the field oxide layer comprises silicon oxide.

Regarding claim 8, Scott et al discloses on figure 6 the integrated circuits further comprise complementary metal oxide semiconductor integrated circuits.

Regarding claims 17-18, Scott et al discloses on figure 6 the field oxide layer 22 has an uppermost side, said metal plug 26 being disposed on said uppermost side of said field oxide layer.

Regarding claims 21-22, Scott et al discloses on figure 6 said metal plug 26 contacts field oxide layer 22.

Claims 9-16, 19-20, 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Deboer et al.

Regarding claim 9, Deboer et al discloses on figure 5 a semiconductor device adapted to prevent and/or thwart reverse engineering comprising "field oxide [16] disposed on a semiconductor substrate; a metal plug contact [39] disposed outside a contact region and above said field oxide layer; and a metal [60] connected to said metal plug contact".

Regarding claim 10, Deboer et al discloses on figure 5 the semiconductor device comprises integrated circuit.

Regarding claim 11, Deboer et al discloses on figure 5 the field oxide layer comprises silicon oxide.

Regarding claim 12, Deboer et al discloses on figure 5 the integrated circuits further comprise complementary metal oxide semiconductor integrated circuits and bipolar integrated circuits.

Regarding claim 13, Deboer et al discloses a method for preventing and /or thwarting reverse engineering comprising steps of "providing a field oxide layer [16] disposed on a semiconductor substrate; providing a metal plug contact [39] disposed outside a contact region and above said field oxide layer; and connecting a metal [60] to said metal plug contact".

Regarding claim 14, Deboer et al disclose a method on figure 5 the semiconductor device comprises integrated circuit.

Regarding claim 15, Deboer et al discloses on figure 5 the field oxide layer comprises silicon oxide.

Regarding claim 16, Deboer et al discloses on figure 5 the integrated circuits further comprise complementary metal oxide semiconductor integrated circuits.

Regarding claims 19-20, Deboer et al discloses on figure 5 the field oxide layer 16 has an uppermost side, said metal plug 39 being disposed on said uppermost side of said field oxide layer.

Regarding claims 23-24, Deboer et al discloses on figure 5 said metal plug 39 contacts field oxide layer 16.

Claims 1-3, 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sur, Jr., et al.

Regarding claim 1, Sur, Jr., et al discloses on figure 13 a semiconductor device adapted to prevent reverse engineering comprising "field oxide layer [12] disposed on a semiconductor [10]; a metal plug contact [36] disposed within a contact region and above said field oxide layer; and a metal [38b] connected to said metal plug contact".

Regarding claim 2, Sur, Jr., et al discloses on figure 13 the semiconductor device comprises integrated circuit.

Regarding claim 3, Sur, Jr., et al discloses on figure 13 the field oxide layer further comprises silicon oxide.

Regarding claim 5, Sur, Jr., et al discloses on figure 13 a method for preventing reverse engineering comprising steps of "providing a field oxide layer [12] disposed on a semiconductor substrate [10]; providing a metal plug contact [36] disposed within a contact region and above said field oxide layer; and connecting a metal to said metal plug contact".

Regarding claim 6, Sur, Jr., et al discloses on figure 13 the semiconductor device comprises integrated circuits.

Regarding claim 7, Sur, Jr., et al discloses on figure 13 the field oxide layer further comprises silicon oxide.

Claims 9-16, 19-20, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Chuang.

Regarding claims 9-16, 19-20, 23-24, Chuang discloses on figure 2I all the structures set forth in the claimed invention.

R sponse to Arguments

Applicant's arguments filed on 9/16/2002 have been fully considered but they are not persuasive.

With respect to claims 1, 5, applicant argues that Scott et al fails to disclose, "a metal plug contact disposed...above said field oxide layer". However, Scott et al clearly discloses on figure 6 a metal plug contact 26 is disposed above a layer of silicide 20, which is above the filed oxide 22. Therefore, the metal plug contact 26 is clearly disposed above the field oxide layer 22. Further, Scott et at discloses on figure 6 the metal plug contact 26 is disposed on the uppermost side of the field oxide layer 22. Note that the metal plug contact 26 is in contact with the uppermost side of the field oxide layer 22, and thus the metal plug contact is disposed on the uppermost side of the field oxide layer in a broad sense. Note that the contact region is the portion where the metal contact plug and metal layer are located in figure 6 of Scott et al. Applicant fails to structurally define a so-called contact region in a distinct manner as such the contact region of the claimed invention does not distinguish from that of Scott et al reference.

With respect to claims 1, 5, applicant argues that Sur, Jr. et al fails to disclose the metal plug contact is disposed above the field oxide layer. However, Sur, Jr. et al discloses on figure 13 the metal plug contact 36 is disposed on the field oxide layer 12.

Applicant's arguments with respect to claims 9-16, 19-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
October 31, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800